

IDS #0304

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

Sheet

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of

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Application Number	10/624,794
Filing Date	July 22, 2003
First Named Inventor	Juha Mikko Hakkarainen
Art Unit	Unassigned 2826
Examiner Name	Unassigned Pert
Attorney Docket Number	55123P256

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.*	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
EP		BEHZAD RAZAVI, <u>Design of Analog CMOS Integrated Circuits</u> , pgs. 619-627, 637-462 and 650-653, McGraw-Hill Higher Education, ISBN 0071188150, 2001.	
EP		IURI MEHR & LARRY SINGER, <u>A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC</u> , pgs. 318-325, IEEE Journal of Solid-State Circuits, Vol. 35 No. 3, March 2002.	
EJ		<u>Lessons in Electrical Circuits</u> , Vol IV (Digital), Chapter 13, http://www.ibiblio.org/obp/electricalcircuits/digital/digi_13.html , 4/2003.	
EP		B.RAZAVI & B.WOOLEY, <u>A 12-b 5-MSample/s Two-Step CMOS A/D Converter</u> , IEEE Journal of Solid-State Circuits, pgs. 1667-1678, Vol. 27 No. 12, December 1992.	
EJ		THOMAS LEE, <u>The Design of CMOS Radio-Frequency Integrated Circuits</u> , pgs. 37-47, Cambridge University Press, Cambridge, UK, ISBN 0521630614, 1998.	
EJ		D.ALLSTOT & W.BLACK, <u>Technological Design Considerations for Monolithic MOS Switched-Capacitor Filtering Systems</u> , pgs 967-986, Prod. of the IEEE, Vol 71 No 8, August 1983.	
EJ		JAMES L. McCREARY, <u>Matching Properties, and Voltage and Temperature Dependence of MOS Capacitors</u> , pgs. 608-616, IEEE Journal of Solid-State Circuits, Vol. SC-16, No. 6, December 1981.	

Examiner Signature	<i>Eun Pert</i>	Date Considered	<i>4-2-06</i>
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*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Applicant's unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Based on PTO/SB/068 (08-03) as modified by Blakely, Solikoff, Taylor & Zafman (wir) 08/11/2003.
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<i>EP</i>		YANNIS TSIVIDIS & PAOLO ANTOINETTI, <u>Design of MOS VLSI Circuits for Telecommunications</u> , pgs. 20-22, 314-333, Prentice-Hall, New Jersey, ISBN 013200643X01, 1985.	
<i>EP</i>		PAUL R. GRAY & ROBERT G. MEYER, <u>Analysis and Design of Analog Integrated Circuits</u> , Third Edition, pgs. 139-140, 167-170, John Wiley & Sons, Inc., ISBN 0471574953, 1993.	
<i>EP</i>		RAYMOND M. WARNER & JAMES N. FORDEMWAHL, <u>Integrated Circuits Design Principles and Fabrication</u> , pgs. 246-255, 270, McGraw-Hill Book Company, 1965.	
<i>EP</i>		YOUNG-DEUK JEON, SEUNG-CHUL LEE, SANG-MIN YOO, & SEUNG-HOON LEE, <u>Acquisition-Time Minimization and Merged-Capacitor Switching Techniques for Sampling-Rate and Resolution Improvement of CMOS ADCs</u> , pgs. 451-454, 2000 IEEE International Symposium on Circuits and Systems, 5/28-31, Geneva, Switzerland, 2000.	
<i>EP</i>		RICHARD C. DORF Editor-in-Chief, <u>The Electrical Engineering</u> , pgs. 15-33, 11321151, CRC Press, Boca Raton, FL, ISBN 0489301858, 1993.	
<i>EP</i>		DAVID HALLIDAY & ROBERT RESNICK, <u>Physics Part Two</u> Third Edition, 650-674, John Wiley & Sons, ISBN 948012, 1978.	
<i>EP</i>		ALAN B GRENNEN, <u>Bipolar and MOS Analog Integrated Circuit Design</u> , pgs. 712-727, 753-764, 784-791, 825-879, ISBN 0471085294, John Wiley & Sons, Inc., 1984.	

Examiner Signature	<i>Em Perf</i>	Date Considered	4-2-06
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